AMENDMENT TO THE SPECIFICATION

I. Please add the following paragraphs after the paragraph that states "Figure 23 is a drawing labeled 'Summary'" and before the heading "Detailed Description of the Presently Preferred Embodiments":

Figure 24(a) shows three cross-sectional views of layers used to fabricate different embodiments of a memory cell built in accordance with the present invention.

Figure 24(b) is a perspective view of a conductor layer and layer stack used in the fabrication of a memory cell built in accordance with the present invention.

Figure 24(c) illustrates the structure of Figure 24(b) after patterning.

Figure 24(d) illustrates the structure of Figure 24(c) after an additional conductor layer and layer stack have been formed.

Figure 24(e) illustrates the structure of Figure 24(d) after patterning.

Figure 24(f) illustrates the structure of Figure 24(e) after an additional conductor layer and layer stack have been formed.

Figure 24(g) illustrates the structure of Figure 24(f) after another patterning step.

Figure 25 is a perspective view of a cut-away portion of the invented array.

Figures 26A-26H illustrate some of the steps used to fabricate one embodiment of the invented memory.

Figure 26A is a cross-sectional elevation view of an antifuse and semiconductor layer formed during the fabrication of the invented array.

Figure 26B illustrates the structure of Figure 26A after an additional semiconductor layer has been formed.

Figure 26C illustrates the structure of Figure 26B after a conductive layer is formed.

Figure 26D illustrates the structure of Figure 26C after an additional semiconductor layer has been formed.

Figure 26E illustrates the structure of Figure 26D after a masking and etching step.

Figure 26F illustrates the structure of Figure 26E after open spaces left from the etching step have been filled.

Figure 26G illustrates the structure of Figure 26F after a planarization step.

Figure 26H illustrates the structure of Figure 26G after another antifuse layer is formed.

Figure 27 is a cross-sectional elevation view of one embodiment of the present invented array.

Figure 28 is a cross-sectional elevation view of a second embodiment of the invented array.

Figure 29 is a cross-sectional elevation view of a third embodiment of the invented array.

II. Please add the following paragraphs before the last paragraph:

Three-Dimensional Memory Devices

Pillar Three-Dimensional Memory Devices

In one embodiment of the present invention, a conductor layer (say, conductor layer number J) runs north-to-south, and adjacent conductor layers (numbers J-1 and J+1) run east-to-west. Wherever a conductor's vertical projection on layer (J) crosses over a conductor on layer (J-1), a memory cell pillar is created. Similarly, wherever a conductor's projection on layer (J+1) crosses a conductor on layer (J), a memory cell pillar is created. Memory cell pillars are defined and patterned by the intersection (crossover) of the conductors, and so the pillars are selfaligned to the conductors. Selfalignment is an extremely important advantage, because it lets the photolithographic patterns of the memory cell be designed without including any extra allowance for misalignment tolerances. Thus the pattern features of our selfaligned memory cell may be made smaller, resulting in a smaller cell area, which gives higher density and lower cost.

For purposes of illustrating the selfaligned fabrication of these pillars, consider an embodiment which uses four sequential layers of material (a "layer stack") to fabricate the steering element and the state change element. In this illustrative example the steering element consists of a polycrystalline silicon PN junction diode, and the state change element consists of a poly-oxide-poly dielectric rupture antifuse. Other embodiments are set forth in the body of this application.

In this embodiment, a pillar contains four layers of material in a layer stack, deposited sequentially as shown in FIG. 24(a): (1) a layer of P+doped polysilicon 40; (2) a layer of N-doped polysilicon 41; (3) a layer of silicon dioxide 42; (4) a layer of N+ doped polysilicon 43.

Layers (40) and (41) form a PN junction diode (the steering element), and layers (41-43) form a poly-oxide-poly dielectric rupture antifuse. In this embodiment the stack of four materials which together create the memory cells are referred to as the "layer stack" 45. There are also a conductor layer below and above the layer stack 45 which is patterned as will be described. These are shown as conductors 46 and 48 in FIG. 24(a).

An alternate stack is shown in FIG. 24(a) as stack 450. Again it includes conductors at the ends of the stack, specifically 460 and 480 which may be fabricated from any conductive material such as a metal or a polysilicon. The steering element in stack 450 comprises a first layer 400 of P+ doped semiconductor such as microcrystalline silicon, and a second layer 410 of N doped semiconductor such as microcrystalline silicon.

The state change element comprises the layer 420. Layer 420 may be an amorphous silicon layer used to form an antifuse. This layer has a nominal high resistance, however, after a large current is passed through it for programming, its resistance will be substantially lower. The layer 430 is shown as an N+ layer to provide good electrical contact to the overlying conductor 480. Layer 430 could be amorphous, microcrystalline or polysilicon but the processing methods need to be low temperature to maintain the amorphous structure in layer 420.

Another stack 405 is also shown in FIG. 24(a). It comprises an N-polysilicon layer 400, a silicon dioxide layer 402 and an N+ polysilicon layer 403. Again, the layers 400 or 403 could be microcrystalline or amorphous semiconductor layers. The stack 405 is sandwiched between the conductors 406 and 408. Here the steering element is a Schottky diode formed by the metal of conductor 406 and the layer 400. The state change element is an antifuse formed by layer 402. By way of example, layers 406 and 408 may be titanium silicide or aluminum with a thickness of

approximately 1000 A. The layers 400, 402 and 403 may be 500 A, 80 A, and 500 A in thickness, respectively.

The fabrication sequence for the memory cell is schematically illustrated in FIGS. 24(b)-12(g). After deposition and before patterning, the layer stack 45 (or the stacks 450 and 405) is a continuous sheet that extends across the entire integrated circuit (indeed across the entire wafer) such as shown in FIG. 24(b). Conceptually the selfalignment method is a two-etch-step procedure: In the first etch step, this layer stack (a continuous sheet) is patterned into long straight strips running (say) east-to-west, by etching them with the same patterning step that etches the east-to-west conductors on the conductor layer below. After deposition and planarization of an interlevel dielectric, a second conductor and layer stack is deposited. This stack is patterned into long straight strips running north south. Etching used to pattern the north-to-south lines continues until the first layer stack has also been etched through the steering element. This results in pillars formed on the east-to-west running lines. The resulting pillars are perfectly aligned to both the conductor below and the conductor above since both the pillars and the conductors are etched simultaneously. In alternate embodiments the semiconductor layers within the layer stack (45 or 450 or 405) may be deposited as microcrystalline or polycrystalline, and then laser treated to improve crystallinity and enhance the dopant activation.

The cross-section of the pillar will be rectangular with one dimension being equal to the width of the bottom conductors and the other dimension equal to the width of the top conductors. If these conductors have equal width then the cross-section will be square.

The patterning in both east-to-west and north-to-south uses well-known photolithographic steps widely used in the semiconductor industry and may use either wet or dry etching. Also, the

silicon used in the cells and when used for the conductors may be doped insitu or after being deposited, for example, by ion implantation.

Of course other patterning technologies may be used rather than etching, for example "liftoff" technology or "Damascene" technology or an additive rather than subtractive patterning technology may be employed instead of etching. But ideally the layer stack should be patterned in two separate steps, once with the mask that defines the conductors below, and again with the mask that defines the conductors above. This holds true regardless of the specific fabrication techniques used to pattern the various layers.

In practice a large number of vertically stacked memory cells are built, and each conductor layer is selfaligned to both the layer stack below, and the layer stack above. Therefore the etching steps which selfalign the conductors to the pillars, must etch away material from three different layers: the layer stack above, the conductor layer, and the layer stack below.

The processing may begin with a wafer that may have received prior processing steps, for example, CMOS transistors may be fabricated in the monocrystalline substrate for the peripheral circuitry. An insulator then is deposited, and preferably, planarized (using chemical-mechanical polishing ("CMP"), resist etchback planarization, or any of a number of other technologies for planarization). The first conductor layer is deposited such as layer 46 of FIG. 24(b), and then the first layer stack 45 is deposited. FIG. 24(b) shows the wafer at this stage.

Next, the mask which defines the features on the conductors1 layer is applied, and these features are etched into both the pillar layer stack 45 and the conductors1 layer 46 below. An insulator is deposited on the wafer and planarized, using CMP or other planarizing technology. FIG. 24(c) shows the wafer at this stage. Note in particular that the pillar layer stack and bottom layer have, been etched into long continuous strips (46a and 45a) and (46b and 45b), not isolated

individual pillars. Also note that the edges of the pillar layer stack 45a and 45b are aligned to the edges of the conductor 46a and 46b layer, since both were etched at the same time with the same mask. Note the conductors generally comprise coplanar conductors, such as aluminum or other metals, silicides, or doped silicon conductors, for each level.

While not shown in FIG. 24(c) or the other figures, the dielectric fills the voids between the strips (and pillars) and thus adds support to the array. Also it should be noted that the planarization must reveal the upper surface of the strips so that the conductor layer that follows contacts the strips. The planarized dielectric also forms the layers through which the vias and vertical conductors of FIG. 13 in U.S. Patent No. 6,034,882 pass.

Next, the second conductor layer 50 ("conductors2") is deposited, and the second pillar stack 51 ("stack2") is deposited. FIG. 24(d) shows the wafer at this stage. Note that the planarization automatically gives a selfaligned contact between a pillar layer stack (such as 45b) and the subsequent conductor layer (such as 50) above it.

Now, the conductors2 mask is applied, and its features are etched downward into three distinct strata: pillarstack2 (51), conductors2 layer 50, and pillarstack1 (45a and 45b). (This etch stops below the steering element within 45a and 45b., providing a unique circuit path through the memory cell). An insulator is deposited on the wafer and planarized (using CMP or other means). FIG. 24(e) shows the wafer at this stage. Note that the conductors2 mask+etch has completed the definition of the individual pillars (45a 1, 45a 2, 45b 1 and 45b 2) in the layerstack1. Also note that these pillars in the layerstack1 layer are aligned to both the conductors1 layer (46a, 46b) and to the conductors2 layer (50a, 50b), thereby achieving the goal of selfalignment.

Next, the third conductor layer 52 ("conductors3") is deposited, and the third pillar layerstack 53 ("layerstack3") is deposited. FIG. 24(f) shows the wafer at this stage.

Now, the conductors3 mask is applied, and its features are etched downwards into layers stack3, conductors3, and stack2. (This etch stops below the steering element of layer stack 2 and is intended to leave the conductor2 layer intact.) An insulator is deposited on the wafer and planarized (using CMP or other means). FIG. 24(g) shows the wafer at this stage. The conductors3 mask+etch has completed the definition of the individual pillars in the layerstack2 layer (such as 51a 1, 51a 2, 51b 2). FIG. 24(g) shows that (N+1)=3 conductor layers and hence (N+1)=3 masking steps, are required to pattern (N=2) layers of pillar layerstack (not counting the interlevel via layers which are used in the peripheral circuits but not in the memory array). The wafer is now ready to receive more stack layers and conductor layers, at the discretion of the manufacturer.

In one possible embodiment of an array of the invented memory cells the pillars are vertically stacked directly above one another as illustrated in FIG. 24. Note that pillars are lined up in vertically aligned stacks. However, because of selfalignment, this vertical stacking of pillars directly above one another is not a requirement.

Memory cell pillars are automatically formed wherever a conductor on conductor layer (J+1) crosses over a conductor on conductor layer (J). This is true even if the conductor layers are not lined up directly above one another, giving vertical stacks of pillars. In fact it may be preferred that the pillars not be stacked vertically; that is they are offset from one another, as illustrated in FIG. 7 in U.S. Patent No. 6,034,882. Compare FIG. 5 (vertical stacks of pillars) to FIG. 7 in U.S. Patent No. 6,034,882 (pillars offset from one another) to see the effect. Offset or staggered pillar placement such as shown in FIG. 7 in U.S. Patent No. 6,034,882, may be

advantageous in practice. It may help give a smoother wafer surface, more suited to planarization and polishing.

In the foregoing sequence of steps, electrode or conductor material is etched along with device material. Since most plasma metal etches also etch polysilicon, a practical combination of materials that enables such dual etching would be aluminum and polysilicon, for example. Control of the etching process may be effected, if desired, through the use of etch chemistries that are selective (e.g., preferentially etching polysilicon, but stopping on aluminum), or through the use of barrier materials that are not etched by the etchants that remove electrode and device material. The state change element may also be used as an etch stop, particularly if it is an oxide rupture type.

Refractory metals such as molybdenum and tungsten are compatible with conventional CVD deposition temperatures for Si and may be used for the conductors. Metal silicides are compatible with even higher temperatures used to activate dopants in Si. Even heavily doped Si itself can be used as a conductor. The choice may be dictated based on resistivity and integration concerns including etch characteristics.

The planarization described after the first half-step of the foregoing is necessary to form self-aligned contacts to the half-etched cells (i.e., the lines running in the east-west direction in the foregoing example). Such planarization may be effected through a variety of means well known in the art, such as chemical-mechanical polishing (CMP), etched-back spin-on dielectric layers, and etched-back spin-on polymers, to cite three well-known examples. To tolerate the possibility of excessive over-polishing or over-etching that may occur during planarization, a second planarization may be performed after deposition of an electrode layer to insure a planar electrode surface for subsequent deposition of device material layers.

The foregoing process sequence exploits self-alignment to reduce the required alignment tolerances between the pillar and the conductors. This embodiment may be substituted with an embodiment involving one or more additional photomasking steps to explicitly define the pillar itself, rather than defining it using the intersection of two conductor photomasking steps, as is done in the self-aligned process. This may be advantageous in various processes that could exploit the explicitly defined sidewalls that would result from such a process. For example, solid-phase crystallization of amorphous silicon could be used to form the steering element layer stack. The free energies of the sidewalls would be expected to favor the formation of a single crystal or grain within the steering element, which may be advantageous in some system embodiments.

Another process that could exploit explicitly defined sidewalls is laser-induced crystallization. Again, the free energies of the sidewalls would be expected to favor the formation of a single crystal or grain within the steering element.

In processes involving the explicit definition of the pillar, a photomasking step would be used to define a bottom conductor. This would be etched. Then, the layer stack required to form the state change and steering elements would be deposited. Another photomasking step would be used to define the pillar, which would be etched. After this etch, an insulating material would be deposited and planarized as in the self-aligned cell, exposing the top of the pillar to form a self-aligned contact. The top conductor would then be deposited and the process would be repeated for subsequent levels of cells as required.

The order of masking steps in the above process could also be reversed. For example, the pillar could be formed prior to patterning the bottom conductor. In this process, the entire layer stack for the bottom conductor, the steering element, and the state change element would be

deposited. The pillar would then be lithographically defined and etched down through the steering element. The bottom conductor would then be defined and etched. This structure would be passivated using a planarized insulator contacting scheme, as described above. In all three processes, the self-aligned contact could also be replaced by an explicit contact forming photomasking step.

The various device fabrication steps may result in the presence of residual chemicals or dangling bonds that may degrade device characteristics. In particular, device leakage can result from the presence of such dangling bonds or chemicals (e.g., incompletely removed photoresist). A low-temperature (e.g., <400C.) plasma oxidation exposure may be used to grow a clean-up oxide on the edges of the device pillar, thereby passivating edge traps. The growth of the oxide is self-limiting because the oxygen species diffuse only slowly through previously grown oxide, resulting in extremely uniform oxide thickness and, therefore, improved manufacturability. (Plasma oxidation may also be used to form an anti-fuse layer.) Oxide deposition may also be used to passivate the surface, for example, either alone or in conjunction with a grown oxide.

Because, in the foregoing for some embodiments, device material (e.g., polysilicon) is deposited after electrode material (e.g., metals), it is desirable to deposit and process the device material at the lowest practical temperatures to widen the selection of suitable metals. As an example, insitu doped polysilicon may be deposited at low temperatures using LPCVD (low pressure chemical vapor deposition), PECVD (plasma-enhanced chemical vapor deposition), PVD (physical vapor deposition), or UHVCVD (ultra high vacuum chemical vapor deposition). An alternative is to deposit undoped polysilicon, followed by doping and activation using a low temperature process. (Traditional activation steps such as long thermal anneals expose the wafer to potentially unacceptably high temperatures.) It may also be desirable in some cases to

substitute microcrystalline or amorphous silicon or crystallized amorphous silicon for the polysilicon to enable low temperature fabrication.

Another concern is the possibility of diffusion of electrode material (e.g., metal) into the device layer during processing. Low temperature processing helps to reduce the severity of this problem, but may be insufficient to solve it completely. To prevent this problem, a number of barrier materials may be employed. Examples include titanium nitride (TiN), tantalum (Ta) or tantalum nitride (TaN), among many that are well known to the art.

In one embodiment of the cell, a thin dielectric layer is employed as an antifuse element. In such a cell, good uniformity of dielectric thickness, as well as a low film defect density (e.g., of pinholes in the dielectric) are among highly desirable properties. The quality of the dielectric may be enhanced through a variety of means, such as rotating (continuously or periodically) the substrate and/or source during deposition; forming the dielectric by thermal means using plasmas or low-temperature growth chemistries; or by employing liquid-phase dielectric deposition means.

It is desirable to reduce the number of masking steps that involve critical alignment tolerances. One method for reducing the number of masking steps is to employ vias that interconnect several electrode layers. The vias may be rectangular, rather than square, to allow a relaxation in alignment tolerances. For example, to interconnect metal lines in several layers running in the x-direction, the x-edge via size may be made substantially looser than the pitch of the x-lines in the y-direction, resulting in a rectangular via. Vias are discussed in conjunction with FIGS. 12 and 13 in U.S. Patent No. 6,034,882.

Rail-Stack Three-Dimensional Memory Devices

OVERVIEW OF THE STRUCTURE OF THE INVENTED MEMORY ARRAY

The invented memory array is fabricated on several levels and, for instance, may have eight levels of storage. Each level includes a first plurality of parallel spaced-apart rail-stacks running in a first direction and a second plurality of rail-stacks or conductors (depending on the embodiment) running in a second direction. Generally, the first rail-stacks run perpendicular to the second conductors/rail-stacks and hence form a right angle at their intersections. (In the invented array as well as in the prior art, conductors at one level are shared with the next level, hence the term "level" may not be precisely descriptive.)

The use of rail-stacks is a departure from prior art three-dimensional memories where conductors alone were used in lieu of rail-stacks, and where discrete cells (e.g., pillars) were formed at the intersections of the lines. As will be seen, a bit is stored at each of the intersections of rail-stacks. However, there is no apparent individual memory cell at the intersections, rather memory cells are defined by the rail-stacks and intermediate layers. This makes it easier to fabricate the invented array as will be seen. When the array is fabricated all the bits are in the zero (or one) state and after programming, the programmed bits are in the one (or zero) state.

In the embodiment Figure 25 several rail-stacks are illustrated in the partial cross-section of the invented array. For instance, rail-stack 1600 is shown at one height and a half rail-stack 1800 is shown at a second height above the first height. Also, half rail-stacks are disposed between rail-stack 1600 and a substrate 1000. These lower rail-stacks run in the same direction as the half rail-stack 1800. A bit is stored at the intersection of rail-stacks and, for instance, a "cell" is present between the rail-stacks and layers shown within the bracket 1700 and another within the bracket 1900. Each of these brackets span a memory level.

The array is fabricated on a substrate 1000 which may be an ordinary monocrystaline silicon substrate. Decoding circuitry, sensing circuits, and programming circuits are fabricated in one embodiment within the substrate 1000 under the memory array using, for instance, ordinary MOS fabrication techniques. (These circuits may also be fabricated above the substrate.) Vias are used to connect conductors within the rail-stacks to the substrates to allow access to each rail-stack in order to program data into the array and to read data from the array. For instance, the circuitry within the substrate 1000 may select rail-stack 1600 and the rail stack 1800 in order to either program or read a bit associated with the intersection of these rail-stacks. (In the case of the embodiments of Figure 29 some conductors are not part of rail-stacks; these conductors are also coupled to the substrate circuits.)

As shown in Figure 25, an insulating layer 1200 is formed over the substrate in order that the array may be fabricated above the substrate. This layer may be planarized with, for instance, chemical-mechanical polishing (CMP) to provide a flat surface upon which the array may be fabricated.

Following this, a conductive layer 1400 is formed on the substrate. As will be seen, conductive layers are used within the rail-stacks and these layers and the resultant conductors may be fabricated from elemental metals such as tungsten, tantalum, aluminum, copper or metal alloys may be used such as MoW. Metal silicides may also be used such as TiSi2, CoSi2 or a conductive compound such as TiN, WC may be used. A highly doped semiconductor layer such as silicon is also suitable. Multiple layer structures may be used selecting one or more of the above.

Following the deposition of a conductive layer, a layer of semiconductor material (layer 1500) such as silicon is formed over the conductive layer. This is typically a polysilicon layer,

however, an amorphous layer may be used. Other semiconductor materials may be used such as Ge, GaAs, etc. In the embodiment of Figure 25 this semiconductor layer is highly doped and, as will be seen, forms one-half a diode. After masking and etching steps, half rail-stacks are formed. These rail-stacks are "half" or partial rail-stacks since they are approximately half the thickness of the rail-stacks used in the next level.

Following this, in the embodiment of Figure 25, a material for the antifuses used to program the array is deposited. In one embodiment, the layer 2000 is a dielectric such as silicon dioxide which is deposited by chemical vapor deposition (CVD) in a blanket deposition over the half rail-stacks and a dielectric fill, filling the space between the rail-stacks. In another embodiment the layer 2000 is grown on the upper surface of the silicon layer 1500 and only exists on the rail-stacks.

Now a full set of memory array rail-stacks is formed on the layer 2000. This comprises first the deposition of a lightly doped silicon layer 2100 doped with a conductivity type dopant opposite to that used for the silicon layer 1500, a heavily doped silicon layer 2200 doped also opposite to the layer 1500, a conductive layer 2300 and a heavily doped silicon layer 2400 doped with the same conductivity type dopant as layers 2100 and 2200. After masking and etching, the rail-stacks shown in Figure 25, such as rail-stack 1600 are formed. These rail-stacks are, as illustrated, in a direction perpendicular to the rail-stacks above and below them.

While not shown in Figure 25 but as will be described later, the spaces between the rail-stacks after they are defined, are filled with a dielectric such as silicon dioxide. Then the rail-stacks and fill are planarized by CMP. In another embodiment spin-on-glass (SOG) is used to fill the voids, in this case chemical planarization can be used, for example, plasma etching. Other fill and planarization methods can be used.

After formation of the rail-stacks another antifuse layer 2600 is formed, for instance, from a dielectric such as silicon dioxide, silicon nitride, silicon oxynitride, amorphous carbon or other insulating materials or combinations of materials. (Also an updoped layer of silicon may be used for the antifuse layer.)

Now another layer of rail-stacks are defined and only half rail-stacks are shown in Figure 25 at this upper level. This half rail-stack comprises a silicon layer 2800 doped with a conductivity type dopant opposite to that of layer 2400. This is a lightly doped layer. Another silicon layer 3000 is formed on layer 2800 and this layer is doped with the same conductivity type dopant as layer 2800, however, it is more heavily doped. Then a conductive layer 3100 is formed above the layer 3000.

Half rail-stacks are used at the very upper-most level of the array and at the very lowest level of the array. In between the half rail-stacks the full rail-stacks, such as rail-stack 1600, are used throughout the array.

It should be noted that the silicon layers disposed on the conductive layers extend the entire length of the rail-stacks in the embodiment of Figure 25 and are uninterrupted except possibly where vias are used to provide a conductive path to the substrate 1000.

In Figure 25 a path 3200 is illustrated from a lower conductor in level 1700 to an upper conductor in this level found in the rail-stack 1800. This path is accessed in one embodiment through decoding circuitry in the substrate for both programming and reading of data into and from the array for one bit.

For instance, to program the bit, a relatively high voltage, 5-20V is applied between the conductors generally so as to forward-bias the "diode" between these conductors. This relatively high voltage causes a breach in the layer 2600 creating a diode. Without this high voltage, the

layer 2600 remains an insulator. Thus, by selecting pairs of conductors, diodes can be selectively formed so as to program the array. While programming the array with the layers adjacent to the antifuse material being forward-biased is currently preferred, it is also possible to program using a reverse-biasing potential.

To sense the data programmed into the array, a voltage lower than that for programming is used. This voltage is applied so as to forward-bias the diode of the cell being accessed and thus allowing a sense amplifier to determine whether or not the layer 2600 is intact between the rail-stacks. Note that "sneak" or parasitic paths in the array which would interfere with the sensing will include a reverse-biased diode.

EMBODIMENT OF FIGURE 27

In the cross-section elevation view of Figure 27, one embodiment is illustrated which corresponds to the embodiment shown in Figure 25. In Figure 27 the half rail-stacks of Figure 25 are not illustrated. Three complete levels 3500, 3600 and 3700 of the array are illustrated in Figure 27. Below layer 3800 of Figure 27 other rail-stacks or half rail-stack are used. Also above layer 6500, a full or half rail-stack is used.

The rail-stack 3 comprising layers 3800 through 4100 includes a lightly doped n- layer 3800, a heavily doped n+ layer 3900, a conductor layer 4000 and n+ layer 4100. The fabrication of these rail-stacks will be discussed in more detail in conjunction with Figure 26A through Figure 26G. An antifuse layer 4200 which for the embodiment of Figure 27 is a blanket deposition covers all of the rail-stacks formed below layer 4200 as well as the fill filling the voids between the rails. As mentioned, the layer 4200 is a deposited silicon dioxide layer in one embodiment.

It should be noted that n+ layers sandwich the conductor layer 4000. These highly doped layers provide ohmic transitions to prevent unintended Schotky formation.

The layers above and below conductor 4000 are not symmetrical for the embodiment illustrated in that an n- layer 3800 is used below the conductor 4000 and not above the conductor 4000. Only a single lightly doped layer (in conjunction with a heavily doped layer) is needed to define a diode; the thickness of this lightly doped layer is important in controlling the break-down voltage and resistance of the diode so formed. The layer 4100, a heavily doped semiconductor layer, and the fill are planarized after the rail-stacks are defined and then a blanket deposition of the antifuse layer 4200 is formed on the layer 4100. (The lines 4300 in Figure 27 are used to indicate that the antifuse layer 4200 and like layers are not etched with the rail-stack below it and thus extend over the entire array for the illustrated embodiment.)

One advantage to the layer 4200 and the other like layers in the structure, such as layers 5100, 5600 and 6500, is that since they are an unbroken deposition, sidewall leakage (into the rail-stacks below) will be minimized, limiting electrical problems during reading and writing. When subsequent conductive material is deposited, it is unable to reach the sides of the rail-stacks below it because of this blanket deposition of the antifuse layer. For instance, path 4900 which would allow silicon from layer 5200 to cause a parasitic path does not exist because of the unbroken blanket deposition of the antifuse layer 5100.

Rail-stacks 4 comprising layers 4400, 4500, 4600 and 4700 are formed on the antifuse layer 4200. Layer 4400 is lightly doped with a p-type dopant for the embodiment illustrated followed by a p+ layer 4500, a conductive layer 4600 and a p+ layer 4700. After these layers are deposited, they are masked and etched to define the rail-stacks. Then the voids between these rail-stacks, such as void 5000, are filled with a dielectric. The fill dielectric is planarized along

with a portion of p+ layer 4700. Planarization is done at this point in the fabrication since there is generally poor control over the thickness and contour of the fill. The fill tends to build up on the rail-stacks when a non-spin-on deposition is used. This is followed by a blanket deposition of layer 5400.

The process is now repeated this time beginning with an n- layer 5200 followed by an n+ layer 5300, a conductive layer 5400 and n+ layer 5500. Again after defining the rail-stacks 5, the voids are filled and the surface is planarized. Another antifuse layer 5600 is deposited. The process is repeated for the rail-stacks 6 this time beginning with a p- layer 6100, p+ layer 6200, conductive layer 6300, p+ layer 6400. Again after defining the rail-stacks, filling the void 6000 and then planarizing, another antifuse layer 6500 is deposited.

As shown by the path 6600, when a large enough voltage is applied between conductors 4600 and 5400 the antifuse layer 5100, at the intersection of layers 4700 and 5200 is breached creating a diode at the intersection. As mentioned, this is selectively done throughout the array to program the array. The conductor 5400 is therefore a bit line for the "cells" above and below it, for instance path 6700 indicates another possible current path for another "cell" where the conductor 5400 is again a bit line during sensing.

It should be noted that with the reversal of the p- and n- layers at each successive rail-stack, planarization always occurs on a heavily doped layer such as layer 4700 and layer 5500. Moreover, the lightly doped layers are always formed on relatively planar surfaces, consequently their thickness can be more easily controlled. This, as mentioned, allows the characteristics of the diode (once the intermediate antifuse layer is breached) to be more reliably controlled.

PROCESSING FLOW FOR THE EMBODIMENT OF FIGURE 27

The process flow for forming rail-stack 5 of Figure 27 is illustrated in Figures 26A-26H. It will be apparent that the rail-stacks for the other embodiment (Figures 28 and 29) are similarly processed.

First, as shown in Figure 26A an antifuse layer 5100 is deposited. This typically is 50-200Å of silicon dioxide which can be deposited with any one of very well-known processes. Following this, a silicon layer 5200 is deposited which is typically 1000-4000Å thick and formed with a CVD process where a phosphorous dopant is deposited along with the deposition of for instance, the polysilicon semiconductor material or where the dopant is ion implanted following the deposition of the layer. This layer is doped to a level of $5 \times 10^{16} - 10^{18}/cm^3$.

Now, as shown in Figure 26B an n+ layer 5300 is deposited again using CVD. This layer may be approximately 300-3000Å thick and in one embodiment is doped to a level of $>10^{19}/cm^3$.

Throughout this application two adjacent silicon layers are often shown such as layers 5200 and 5300, with different doping. These layers may be formed with one deposition and then using ion implantation step at two different energy levels to obtain the two doping levels.

A conductive layer which may be 500-1500Å thick is formed using any one of numerous well-known thin film deposition process such as sputtering. A refractory metal may be used or a silicide of a refractory metal. Also as mentioned aluminum or copper can be used, or more simply the heavily doped silicon can be the conductor.

Next another semiconductor layer of, for instance, polysilicon approximately 1500-2000Å thick is formed again doped to a level of $>10^{19}/cm^3$. This is shown as layer 5500 in Figure 26D; after planarization its thickness is between 300Å and 2000Å thick.

A masking and etching step is now used to define rail-stacks, such as rail-stacks 6900, 7000 and 7100 shown in Figure 26E. Note that when comparing this view to the view of rail-stack 5 of Figure 27, the view in Figure 26E is taken from the side and consequently shows the individual rail-stacks. An ordinary masking and etching step for instance using plasma etching, may be used. Etchants can be used that stop on the antifuse layer thus preventing this layer from being etched away. Thus, layer 5100 can be considered an etchant stop layer depending on the specific etchants used.

Now as shown in Figure 26F, the spaces between the rail-stacks are filled with a dielectric such as formed with a HDPCVD process.

Chemical-mechanical polishing is then employed to planarize the upper surface of the rail-stacks shown in Figure 26F in one embodiment. Chemical etching can also be used as mentioned with certain dielectrics. This planarization can reduce the thickness of the layer 5500 to approximately 500Å, thus this layer ends up being of approximately the same thickness as the layer 5300.

Next as shown in Figure 26H another antifuse layer 5600 is formed on the planarized surface 7500. Since the layer 5600 is deposited over all the rail-stacks and the filler material and remains unetched, it forms a barrier to the migration of the materials subsequently deposited that might make their way along the sides of the rail-stacks such as along path 7900. Thus the layer 5600 helps prevent the parasitic paths and potential shorts that may occur with prior art memories.

It should be noted that in Figure 27 while the antifuse layer is shown as a blanket layer covering the rail-stacks and fill, it is possible also to fabricate each level where the antifuse layer is in fact grown from a semiconductor layer. For instance, an oxidation step may be used to grow

a silicon dioxide layer from layers 4100, 4700, 5500 and 6400. This grown layer would then be in lieu of the antifuse layers shown in Figure 27.

THE EMBODIMENT OF FIGURE 28

For the embodiment of Figure 28 each rail-stack begins with a conductor such as layer 8000 of Figure 28. An n+ semiconductor layer 8100 and an n- layer 8200 are formed on layer 8000. Next a layer of antifuse material 8300 is formed. Then a p+ layer 8400 of semiconductor material is deposited (e.g., silicon with boron dopant) on the antifuse. When the rail-stacks are formed, for instance for rail-stack 200 of Figure 28, the antifuse layer 8300 is etched as well as layers 8000, 8100, 8200 and 8400.

The voids between the rail stacks are now filled and planarization is done, planarizing the fill with the upper surface of the layer 8400. Following the completion of the rail-stack 2 the next rail-stacks are formed shown as rail-stacks 3 in Figure 28. This comprises a conductor layer 8500, p+ layer 8600, p- layer 8700, antifuse layer 8800 and n+ layer 8900. Again masking and etching occur. This etching also etches the exposed regions of layer 8400 which does not appear in the view of Figure 28, but this will be apparent shortly when region 9500 of the next stack is discussed. Now filling and planarization occurs and the next layer of rail-stacks are formed shown as rail-stack 400. As illustrated, this comprises a conductive layer 9000, n+ layer 9100, n- layer 9200, antifuse layer 9300, and p+ layer 9400. Once again masking, etching, filling and planarization occur.

Unlike the embodiment of Figure 27, when rail-stacks at any particular height are formed, etching must occur on one layer of the rail-stack immediately below the rail-stack being defined. For instance, when rail-stack 4 is etched the layer 8900 of rail-stack 3 is etched away where it is not covered by rail-stack 4 as shown by region 9500. This etching is used to remove all of the

semiconductor material between the adjacent conductors and consequently prevent a path, such as path 9600 shown in Figure 28. This etching also occurs to layer 8400 which, as mentioned, is not seen in Figure 28. In this connection the antifuse layer 8800 can be used as an etchant stop, although this is not necessary. No harm is done if etching does occur through the layer 8800 since the antifuse layer is only needed at the intersections of the rail-stacks. Note the etching of the region 9500 is done in alignment with overlying rail-stacks and consequently no additional masking is required.

As was the case with the earlier embodiment, the order of the n and p doped layers alternate with each successive rail-stack. Moreover, the rail-stacks at any given height include both p and n layers. In contrast, for the embodiment of Figure 27, at any particular height, the rail-stacks are doped with either an n type or p type dopant but not both.

EMBODIMENT OF FIGURE 29

In the embodiment of Figure 29, alternate levels of rail-stacks running in a first direction and intermediate layers of conductors are running in a second direction are used. For instance as shown in Figure 29, the conductors 3, 5 and 7 run in a first direction whereas the rail-stacks 4 and 6 run in a second direction.

In this embodiment each of the rail-stacks is symmetrical about a conductor such as conductor 10900 of rail-stack 4. The conductor is sandwiched between two n+ layers 10800 and 11000. More lightly doped outer layers 10700 and 11100 are disposed on these more heavily doped layers.

In fabrication the conductors such as conductors 10500, are first formed, for instance, on the substrate. The spaces between these conductors may be filled and planarization may occur. Then an antifuse layer 10600, n- layer 10700, n+ layer 10800, conductive layer 10900, n+ layer

11000 and n- layer 11100 are deposited. Rail-stacks are then defined by masking and etching. The voids between the rail-stacks are then filled with a dielectric. Then planarization of the filling material and the upper surface of layer 11100 is performed. Following this, antifuse layer 11200 is deposited over the entire array. Now additional conductors are formed such as conductors 11300. Each level in this array is between a metallic conductor such as conductor 10500, and a sandwich conductor such as conductor 10900. Thus there are four memory levels shown in Figure 29, levels 10000, 10100, 10200 and 10300.

Programming in this array causes the formation of Schottky diodes consequently, the conductors such as conductors 10500 and 11300 must be of a suitable material to allow formation of a Schottky diode. For instance, aluminum and some refractory metal or silicides may be used.

OTHER EMBODIMENTS

In the above description a conductor is shared by two levels. An array may be fabricated where there are two conductors for each level that are not shared with other levels. A dielectric may be used to separate each such level. Also while above diodes on alternate levels "point" in the same direction, this is not necessary. For instance, a shared conductor may have diodes point-in from above and point-out from below. This requires different driving circuitry in the substrate.

III. Please replace the paragraph of the Abstract with the following amended paragraph:

~~This invention is directed to a chip-level architecture used in combination with a monolithic three-dimensional write-once memory array.~~ In one embodiment, a chip-level architecture is provided comprising a monolithic three-dimensional write-once memory array and at least two of the following system blocks: an Error Checking & Correction Circuit (ECC); a Checkerboard Memory Array containing sub arrays; a Write Controller; a Charge Pump; a Vread Generator; an Oscillator; a Band Gap Reference Generator; and a Page Register/Fault Memory. In another embodiment, a chip-level architecture is provided comprising a monolithic three-dimensional write-once memory array, ECC, and smart write. The monolithic three-dimensional write-once memory array comprises a first conductor, a first memory cell above the first conductor, a second conductor above the first memory cell, and a second memory cell above the second conductor, wherein the second conductor is the only conductor between the first and second memory cells.